ABSTRACT OF THE DISCLOSURE

A method and apparatus for an improved timer circuit and improved pulse width detection includes initiating a ramp timer and setting a timer latch output level substantially simultaneously in response to the occurrence of an input signal. The occurrence of the input signal also causes a counter to be enabled to count clock cycles. The ramp timer signal of the ramp timer is frozen (i.e., paused) by a timer control circuit, upon the occurrence of a first clock cycle following the enabling of the counter. The counter then counts a predetermined number of clock cycles after the ramp timer signal is frozen and, upon the occurrence of a last one of a predetermined number of clock cycles, generates a terminal count signal. Upon receiving the terminal count signal, the timer control circuit unfreezes ramp timer signal. The ramp timer runs until completion at which time the ramp timer generates an end of ramp control signal. The control signal is communicated to timer latch to reset timer latch output level.